Gain Partitioning: A New Approach for Analyzing the High-Frequency Performance of Compound Semiconductor FET's

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Abstract—**A new approach for analyzing the high-frequency performance of compound semiconductor FET's is presented. The approach is based on a circuit description that separates intrinsic and parasitic circuit elements of active devices in a general way. Mason's gain (U) and current gain (A_i) have been used to illustrate this approach, since their unity gain frequencies, f_{max} and f_τ, respectively, are good indicators of high-frequency performance. Significant results from U have been related to a more commonly used nomenclature involving maximum stable gain (MSG) and maximum available gain (MAG) and, in particular, to the transition from a potentially unstable device to a potentially stable device. Results presented here show that the requirements to maximize these cutoff frequencies are different. Minimized parasitic circuit elements maximize f_τ. A maximized f_{max}, on the contrary, may be obtained if interactions of parasitic and intrinsic circuit elements satisfy certain conditions. The method presented here should be used in conjunction with software that can specify the physical structure required to realize those circuit elements.**

I. Introduction

THE speed with which a circuit can respond to a signal is determined by the circuit configuration as well as by the number and type of transistors and passive components in the circuit. However, regardless of the choice of circuit configuration and passive components, there are unavoidable speed limitations which depend on the transistor characteristics. It is important to know how the gain characteristics of an amplifier are related to the properties of the available transistors. Recent advances in GaAs compound semiconductor materials and improved technologies have resulted in several novel FET structures. Progress in known technologies has also enhanced, e.g., MESFET devices, allowing them to reach a performance comparable to that of AlGaAs/GaAs HEMT's and AlGaAs/In GaAs pseudomorphic HEMT's for millimeter-wave low-noise and power applications [1], [2]. These results are the first demonstration of the potential volume production of high-performance ion-implanted MESFET's for millimeter-wave application.

Useful power gain from FET's or HEMT's at high millimeter-wave frequencies is difficult to achieve. High-frequency performance depends crucially on the fabrication process. The fabrication difficulties suggest a question: Can we manipulate the various material and structure features of the device to enhance gain performance to reach higher frequencies? Trew [3] gives an affirmative answer to this question and reports that, by varying the delay, Mason's gain near f_{max} can be tuned to obtain an optimized performance. This observation is significant since it indicates that a minimized time delay may not be sufficient to obtain a maximized f_{max}. It does indicate that the device structure may be optimized to obtain a tuned high-frequency response.

In addition, it was shown [5] that an increase of the charging resistance, usually denoted R_i, indicates a possible enhancement of f_{max}. Therefore, to better understand these possible gain–frequency responses, new guidelines in high-frequency modeling are required. More precisely, since parasitic circuit elements cannot be eliminated, there is a need for powerful computer-aided methods that allow the gain of an overall FET to be predicted and analyzed in terms of an active and passive circuit description.

In this paper we present an approach that makes it possible to analyze the overall gain of the transistor and simultaneously observe the interaction of the two separated parts. An important benefit of this approach is that we may avoid introducing simplifications to the network equations. It is important to note that the concept of an equivalent circuit representation is an abstraction and a simplification of a physical device. It gives, however, a way of describing the electrical behavior of the circuit in a proper way. Therefore, once the equivalent circuit is determined, no additional simplification should be introduced. It has been shown how low-frequency approximations can result in erroneous results for high-frequency applications [3]–[5], [8].

II. Methods for Predicting High-Frequency Performance of Compound Semiconductor Transistors

We present here a short review of some contributions which, in this author's opinion, have had a marked influence on the progress in the high-frequency performance of transistors.

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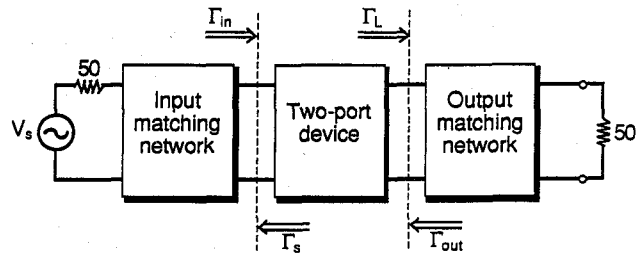

Fig. 1. Conjugate match exists when $\Gamma_{in} = \Gamma_s^*$ and $\Gamma_{out} = \Gamma_L^*$.

A. Mason's Gain

The concept of unilateral gain in linear amplifiers was treated in a classical paper by Mason [9] in 1954. The set of all nonsingular lossless reciprocal transformations forms a group in the mathematical sense. All invariants of the two-port impedance matrix, Z, under that group were found to be related to a basic invariant, which has the form

$$U = \frac{|\Delta(Z - Z^T)|}{\Delta(Z + Z^*)} = \frac{|z_{21} - z_{12}|^2}{4(r_{11}r_{22} - r_{12}r_{21})} \tag{1}$$

where Z^T is the transpose of Z, Z^* is the complex conjugate, and Δ is a determinant. The z_{ij} are the two-port impedance parameters of the device in question and r_{ij} is the real part of z_{ij}. The quantity U was identified by Mason as the available power gain of the resulting amplifier, whose reverse transfer impedance disappears. Therefore, U is called the unilateral gain. When $U = 1$, we obtain a cutoff frequency, usually denoted f_{max}.

B. Maximum Available Gain

A commonly used measure of amplification is the maximum available gain (MAG). For a two-port with the stability factor, k, greater than unity, it is possible to simultaneously conjugate match the two-port to produce the maximum available gain (see Fig. 1).

The maximum available gain can be written as [6]

$$\text{MAG} = \frac{|y_{21}|}{|y_{12}|} \cdot \frac{1}{k + \sqrt{k^2 - 1}} \tag{2}$$

where

$$k = \frac{2\,\text{Re}(y_{11})\,\text{Re}(y_{22}) - \text{Re}(y_{12}y_{21})}{|y_{21}y_{12}|}. \tag{3}$$

In order to arrive at manageable formulas expressed in the equivalent circuit parameters of a device, the MAG is calculated near the frequency limit of the transistor. With the assumption that $k > 2$, the MAG is usually approximated by

$$\text{MAG} \approx \frac{|y_{21}|}{|y_{12}|} \cdot \frac{1}{2k}. \tag{4}$$

This approximate expression was used by Wolf [6]. By using the circuit topology of Fig. 2, Wolf presented a closed-form expression for the cutoff frequency f_{max}, given

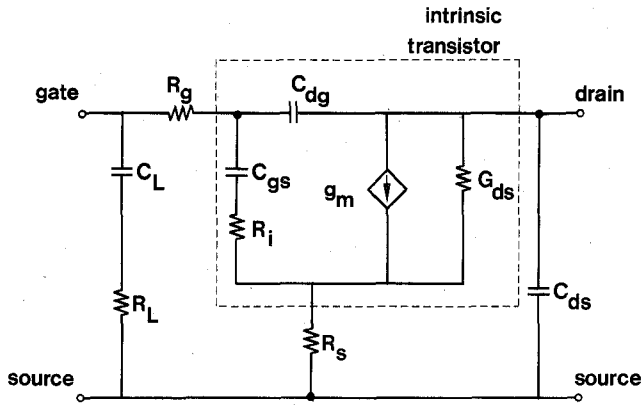

Fig. 2. Circuit elements of a Shottky barrier FET (after Wolf [6]).

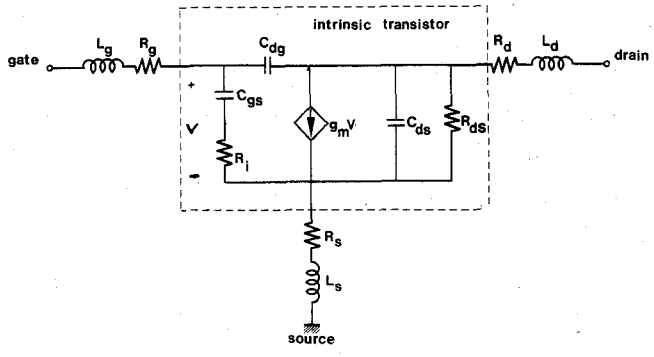

Fig. 3. Equivalent circuit of an FET including parasitic elements (after Ohkawa [7]).

by

$$f_{max} \approx \frac{1}{2\pi} \cdot \frac{g_m}{\sqrt{(4C_{gs}G_{ds}(\tau_i + \tau_s + \tau_g) + 2C_{dg}(C_{dg} + g_m(\tau_t + \tau_s + 2\tau_g)))}} \tag{5}$$

where

$$\tau_i = R_i C_{gs} \tag{6}$$

$$\tau_s = R_s C_{gs} \tag{7}$$

$$\tau_g = R_g C_{gs} \tag{8}$$

and τ_t is the delay in the voltage-controlled current source.

It was recognized by the author that one cannot expect the expression to be accurate since the derivation contains many approximations. However, Wolf claimed that because all important elements of the equivalent circuit are incorporated, the closed-form expression can be helpful in transistor design.

This work was further expanded by Ohkawa *et al.* [7]. By using (4) and the circuit topology of Fig. 3, they developed an approximate expression for the MAG that also included the source inductance, L_s. For the conve-

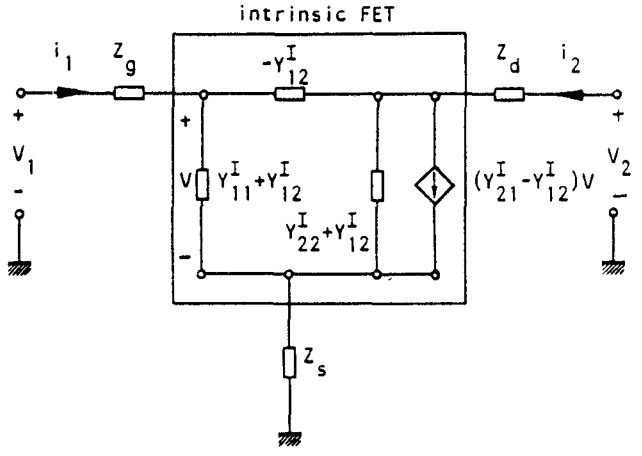

Fig. 4. Partitioning of a single-gate FET into intrinsic and parasitic elements. Parasitic elements are $z_s = R_s + j\omega L_s$, $z_g = R_g + j\omega L_g$, and $z_d = R_d + j\omega L_d$.

nience of the reader their expression is rewritten:

$$\mathrm{MAG} \approx \left(\frac{f_T}{f}\right)^2 \Bigg/ \left(4G_{ds}\left(R_i + R_s + R_g + \frac{\omega_T L_s}{2}\right) + 2\omega_T C_{dg}\left(R_i + R_s + 2R_g + \omega_T L_s\right)\right) \quad (9)$$

where

$$\omega_T = 2\pi f_T = \frac{g_m}{C_{gs} + C_{dg}}. \quad (10)$$

Their work also includes a noise analysis, and important steps in the fabrication process of the FET are clarified.

III. New Method of Analysis

There is a need for device designers to be able to explore the benefits of changing the physical layout of standard compound FET's, e.g. in order to increase the power-handling capability or cutoff frequency. A physical device may be described by an equivalent circuit representation. Therefore, the benefits may be studied by means of basic circuit theory. An accurate formulation should use a realistic circuit description where elements representing the physical processes responsible for device operation should be present. To fulfill these basic requirements the complete circuit topology of Fig. 4 is used and the corresponding intrinsic equivalent circuit is shown in Fig. 5. Several popular circuit models are obtained by deleting elements from this general circuit description.

To obtain a compact and a manageable notation, it is assumed that the S parameters are transformed to the corresponding two-port impedance parameters. A more detailed description, explaining the advantages of using a circuit description in terms of z and y parameters, can be found in [10]. Furthermore, signal levels are assumed to be small enough to make linear analysis valid.

Several measures of gain, for example power gain (G_p), available gain (G_a), maximum available gain (MAG), maximum stable gain (MSG), Mason's gain (U), and current gain (A_i), all with their respective definitions, are important in the design of both complete amplifiers and FET's. However, to approach the concept of gain partitioning, U and A_i are used. Their corresponding unity gain frequencies, $f_{\max}$ and f_τ, are distinct indicators of high-frequency performance.

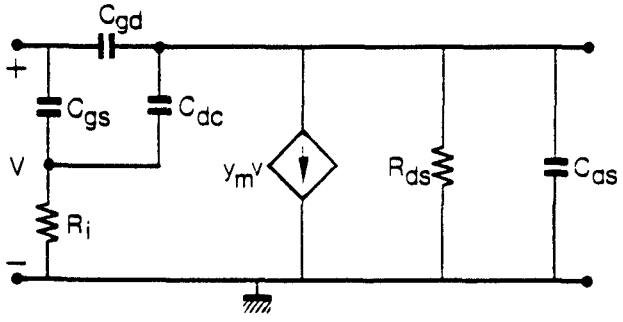

Fig. 5. Intrinsic equivalent circuit $y_m = g_m \exp(-j\omega\tau)$.

Important conditions when mathematically formulating the new method of analysis are as follows:

- U and MAG definitions of $f_{\max}$ are equivalent. A proof can be found in [5]. Analysis should use the quantity U rather than MAG because analysis that makes use of MAG becomes too complicated.
- There should be partitioning of U and A_i in active and parasitic elements.
- The partitioning procedure should try to describe the interaction of parasitic elements and intrinsic elements in real- and/or complex-valued functions in such a way that the corresponding parasitic circuit elements are coefficients in these functions.

A. Partitioning of Mason's Gain, U

A partitioned expression of Mason's gain may be derived as (see Appendix I)

$$U = \frac{U_i}{1 + U_i(p_s + p_{g,d})} \quad (12)$$

where U_i characterizes the intrinsic element part and p_s and $p_{g,d}$ are both parasitic functions. Their relationships to the impedance parameters are

$$U_i = \frac{|z_{21}^i - z_{12}^i|^2}{4\{r_{11}^i r_{22}^i - r_{21}^i r_{12}^i\}} \quad (13)$$

$$p_s = \frac{4R_s(r_{11}^i + r_{22}^i - r_{21}^i - r_{12}^i)}{|z_{21}^i - z_{12}^i|^2} \quad (14)$$

$$p_{g,d} = \frac{4\{R_g(r_{22}^i + R_d + R_s) + R_d(r_{11}^i + R_s)\}}{|z_{21}^i - z_{12}^i|^2} \quad (15)$$

where r_{kl}^i is the real part of z_{kl}^i. The parasitic functions possesses the following properties:

$$p_s = \begin{cases} 0 & \text{for } R_s = 0 \\ < 0 & \text{for } 0 < f \leq f_s; \quad R_s \neq 0 \\ > 0 & \text{for } f > f_s; \quad R_s \neq 0 \end{cases}$$

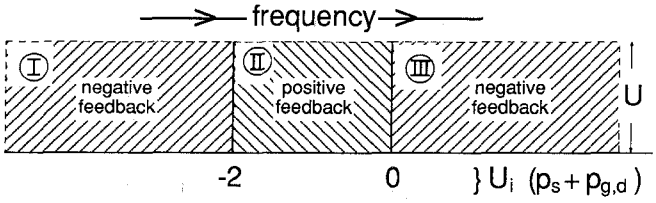

Fig. 6. Possible feedback regions of Mason's gain.

where f_s is a frequency that can be located high in the millimeter-wave region and

$$p_{g,d} = \begin{cases} 0 & \text{for } R_g = R_d = 0 \\ > 0 & \text{for all frequencies.} \end{cases}$$

This makes it possible to illustrate some general properties of (12) (see Fig. 6). It is possible, as frequency increases from left to right along the abscissa, to transit regions of negative feedback → positive feedback → negative feedback, refered to Mason's gain, U. The various feedback regions shown in Fig. 6 explain why U can sometimes show a resonance in the gain–frequency characteristic or merely a -6 dB/octave slope in frequency performance.

It is important to note that a transistor can also have characteristics located only in one or two regions as the frequency varies. To examine this, we take the denominator of (12),

$$U_i(p_s + p_{g,d}) + 1 \tag{16}$$

and see that when

$$U_i(p_s + p_{g,d}) = -1 \tag{17}$$

Mason's gain, U, is in resonance. The frequency for which (17) is fulfilled is hence a critical parameter. From this it is clear that if low-frequency values are satisfied by

$$U_i(p_s + p_{g,d}) \leqslant -1 \tag{18}$$

or

$$U_i(p_s + p_{g,d}) > -1 \tag{19}$$

then the resulting gain–frequency characteristics are different in nature. If (18) is satisfied, U is resonant at some frequency and we have a gain slope of -12 dB/octave after the complex pole pair. In general, (18) suggests that if the left-hand side of (18) is less than -2 at low frequencies, U passes through all three feedback regions. On the other hand, if (19) is satisfied, U can pass through two feedback regions and show a gain slope of -6 dB/octave at low frequencies and -9 dB/octave at high frequencies before cutoff, $f_{\max}$. This is illustrated in subsection III-B.

It would be instructive for the reader if (17)—Mason's gain in resonance—could be related to a more common nomenclature. In fact, (17) is closely related (not mathematically equivalent) to another formulation that uses the scattering parameters and the stability factor, namely the transition from maximum stable gain (MSG) to maximum available gain (MAG). Since there is a loss of -3 dB/octave of the gain–frequency response at the transition MSG → MAG, it can be understood that the corresponding frequency for the transition is critical, in order to obtain a maximized cutoff frequency, $f_{\max}$.

For the case where network parameters of an active device satisfy (19) for all frequencies, it has not been possible to identify a relationship between U and the transition MSG → MAG.

TABLE I
TRANSISTOR DATA USED TO ILLUSTRATE FEEDBACK REGIONS

Device	T1	T2	T3
Parameter (intrinsic)			
$R_i[\Omega]$	7.32	7.32	7.32
$R_{ds}[\Omega]$	206.4	206.4	206.4
g_m[mS]	57.2	57.2	57.2
τ[ps]	3.17	3.17	3.17
C_{gs}[pF]	0.287	0.287	0.287
C_{ds}[pF]	0.082	0.082	0.082
C_{dg}[pF]	0.029	0.029	0.029
C_{dc}[pF]	0.010	0.010	0.010
Parameter (parasitic)			
$R_g[\Omega]$	4.0	2.0	8.0
$R_d[\Omega]$	2.0	8.0	4.0
$R_s[\Omega]$	8.0	4.0	2.0
$f_{\max}$[GHz]	≈ 53	≈ 44	≈ 39
Frequency in GHz when $\lvert p_s\rvert = \lvert p_{g,d}\rvert$	31.5	9.1	not ∃

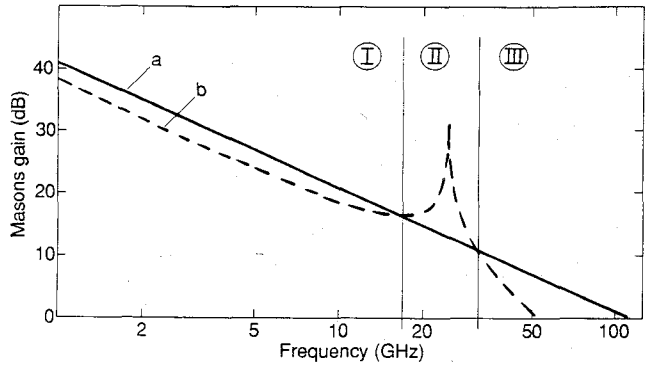

Fig. 7. Mason's gain for transistor T1. *a*: intrinsic gain U_i; *b*: total gain U.

B. Numerical Results for Mason's Gain

In this subsection we clarify the theory with numerical examples. Transistor data are given in Table I and the corresponding gain–frequency characteristics are shown in Figs. 7–10. For clarity, we show each transistor's gain–frequency characteristics in one figure. This simplifies the illustration of the various feedback regions. Note here that transistor T1 passes through all three regions, transistor T2 passes through two regions, and transistor T3 has characteristics located only in one region. Note

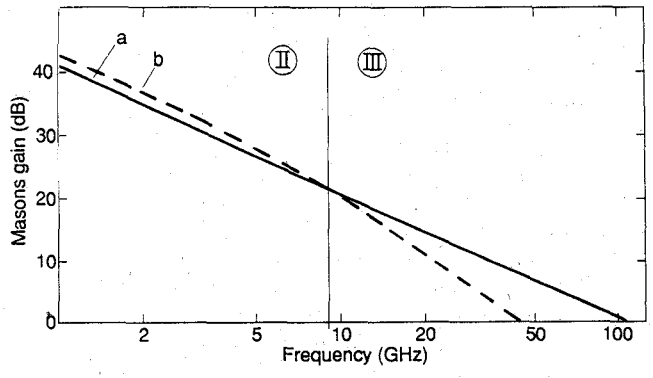

Fig. 8. Mason's gain for transistor T2. *a*: intrinsic gain U_i; *b*: total gain U.

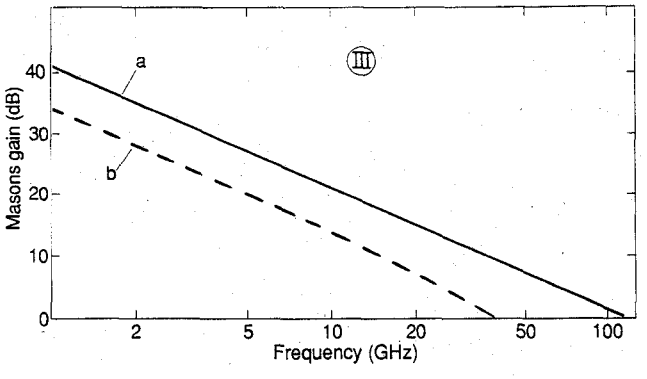

Fig. 9. Mason's gain for transistor T3. *a*: intrinsic gain U_i; *b*: total gain U.

that the element combination $R_g + R_s + R_d = \text{const.}$ for all three transistors.

Circuit models with the topology of Fig. 4 have been developed for various FET's, yielding the element values of Table II. Transistors T4 and T5 both show a resonance in the gain–frequency response and have different cutoff frequencies. Their gain–frequency characteristics are located in all three feedback regions. Transistors T6 and T7 show both a gain slope of -6 dB/octave at low frequencies and a -9 dB/octave at high frequencies before cutoff, $f_{\max}$. Their gain–frequency characteristics are located only in region III. This indicates that if a realistic prediction of high-frequency performance is desired, extrapolations based upon a -6 dB/octave gain slope are not correct.

IV. Partitioning of Current Gain, A_i

A high cutoff frequency, f_τ, in a transistor indicates that it should be useful for integrated logic applications. A convenient way to examine this is to study the current drive capability of the device in question. The current gain of a two-port network is defined as the ratio of output current I_2 to input current I_1 (Fig. 11):

$$A_i = \frac{I_2}{I_1}. \tag{20}$$

Let the two-port device be characterized by a set of

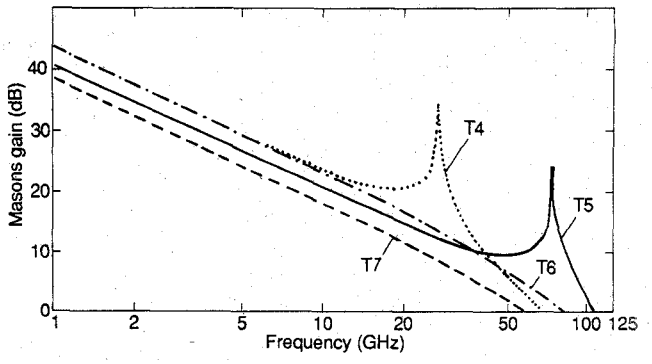

Fig. 10. Mason's gain for the real transistors T4, T5, T6, and T7.

impedance parameters, then it can be shown that the current gain is given by

$$A_i = \frac{-z_{21}}{z_{22} + z_L} \tag{21}$$

and if $z_{22} \neq 0$, A_i may be expressed in terms of hybrid parameters:

$$A_i = \frac{h_{21}}{1 + h_{22} z_L}. \tag{22}$$

For the special case where $z_L = 0$, A_i is called the short-circuit current gain and is often just denoted as h_{21}.

Here, we consider the general case, with $z_L \neq 0$. By using the circuit topology shown in Fig. 4, a partitioned current gain expression may be derived as (see Appendix II)

$$A_i = \frac{(1+a)h^i_{21}}{1 - bh^i_{21}} \tag{23}$$

where

$$a = z_s / z^i_{21} \tag{24}$$

$$b = (z_s + z_d + z_L)/z^i_{21} \tag{25}$$

$$h^i_{21} = -z^i_{21}/z^i_{22} \tag{26}$$

and h^i_{21} denotes the intrinsic current gain.

Interaction of Circuit Elements

In this subsection we present an alternative way of studying the interaction between circuit elements, one different from the analysis applied to Mason's gain in subsection III-A. In this alternative approach we study the denominator of (23), giving particular attention to whether or not the equation $bh^i_{21} = 1$ is satisfied at any frequency of operation. In fact, it can be shown that $bh^i_{21} \neq 1$ for all frequencies. The proof is given below.

Proof: We want to prove that

$$bh^i_{21} \neq 1 \quad \forall \text{ frequencies}. \tag{27}$$

One way to show this is to formulate a proof based on contradiction, i.e., to prove instead that

$$bh^i_{21} = 1 \tag{28}$$

TABLE II
TRANSISTOR DATA FROM REAL DEVICES (†AFTER TREW [4])

Device	T4	T5	T6	T7
Source	Feng [11]	Maki [12]	Lau [13]	Niclas [14]
Structure	$0.3\times150\ \mu$m	$0.25\times60\ \mu$m	$0.5\times100\ \mu$m	$0.35\times200\ \mu$m
Type	MESFET	MESFET	MESFET	MESFET
Parameter (intrinsic)				
$R_i[\Omega]$	0.94	2.69	2.13	3.3
$R_{ds}[\Omega]$	258	556	440	290
g_m[mS]	25.8	15.2	26.0	30.0
τ[ps]	3.0	1.25	0	1.2
C_{gs}[pF]	0.147	0.071	0.104	0.184
C_{ds}[pF]	0.05	0.025	0.020	0.010
C_{dg}[pF]	0.009	0.001	0.016	0.013
C_{dc}[pF]	0.03†	0.011	0.003	0.047
Parameter (parasitic)				
$R_g[\Omega]$	2.9	1.46	2.98	6.4
$R_d[\Omega]$	2.39	6.7	6.55	1.5
$R_s[\Omega]$	2.39	4.55	6.05	0.15
f_{max}[GHz]	66	103.5	79.5	56
Freq. GHz when $\lvert p_s\rvert = \lvert p_{g,d}\rvert$	26.5	71.5	not ∃	not ∃
Feedback regions	I → III	I → III	III	III

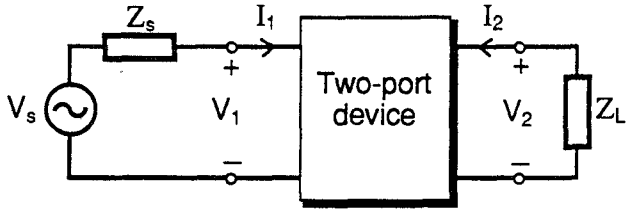

Fig. 11. Terminated two-port network used to illustrate current gain definition.

cannot be satisfied with positive circuit elements. Thus, (28) can be manipulated into the equivalent form

$$\frac{z_{22}^{i}}{z_s + z_d + z_L} = -1. \tag{29}$$

Let $z_{22}^{i} = r_{22}^{i} + jx_{22}^{i}$ and $z_s + z_d + z_L = r_{\text{den}} + jx_{\text{den}}$. Equation (29) can then be expressed as

$$\frac{r_{22}^{i} r_{\text{den}} + x_{22}^{i} x_{\text{den}} + j\left(r_{\text{den}} x_{22}^{i} - r_{22}^{i} x_{\text{den}}\right)}{r_{\text{den}}^2 + x_{\text{den}}^2} = -1. \tag{30}$$

Restricting the imaginary part of (30) to be equal to zero gives

$$\frac{r_{\text{den}}}{x_{\text{den}}} = \frac{r_{22}^{i}}{x_{22}^{i}}. \tag{31}$$

Inserting (31) in (30), we get

$$\frac{r_{\text{den}}}{r_{22}^{i}} \cdot \frac{\left(r_{22}^{i}\right)^2 + \left(x_{22}^{i}\right)^2}{r_{\text{den}}^2 + x_{\text{den}}^2} = -1. \tag{32}$$

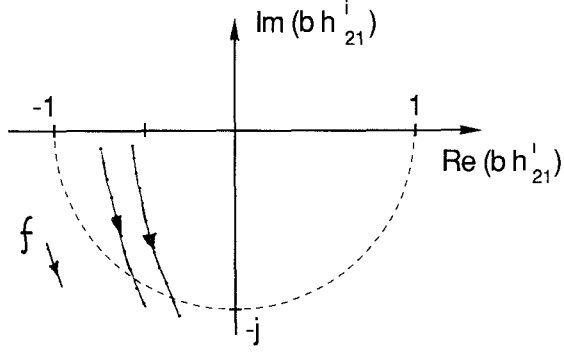

Fig. 12. Typical set to curves characterizing the complex function bh_{21}^{i}.

Equation (32) cannot be satisfied since both $r_{\text{den}} \geq 0$ and $r_{22}^{i} \geq 0$ for all frequencies. Q.E.D.

In addition, it is quite instructive to give some graphical illustrations. Numerical simulations result in the frequency characteristics shown in Fig. 12. These characteristics are typical. It is clear that the frequency dependence of the complex function bh_{21}^{i} does not approach the point where its value is unity.

As the frequency increases, the complex function bh_{21}^{i} departs from the particular solution $bh_{21}^{i} = 1$. Thus, it is clear that the interaction of the two parts cannot force the transfer function of (23) into a region of positive feedback, as in the case for Mason's gain. Any inclusion of parasitic circuit elements degrades the intrinsic gain–frequency response. Therefore, parasitic circuit elements should be minimized, not optimized, to obtain higher cutoff frequencies.

V. Discussion

The speed of active components such as FET's and bipolar transistors is limited by both internal and external circuit components. It is usually recognized among device designers and microwave engineers that in first-order design it is important to maximize g_m and to minimize C_{gs}. Among second-order parameters it is recognized that the internal time delay, τ, is the factor that most limits the speed of the internal components and should therefore be minimized. External components that affect the speed are low-resistance ohmic contacts formed under the drain and source metallization and additional parasitic drain and source resistances. Associated gate resistance and fringing capacitances are other components that affect the high-frequency response.

By using a realistic circuit description that takes into account the series resistances associated with the three terminals of the device, the approach has been applied to two important gain measures, Mason's gain (U) and current gain (A_i). The concept of gain partitioning makes it possible to simultaneously study the interaction of active and parasitic circuit elements. This need cannot be satisfied by using such modern commercial CAD software as TOUCHSTONE and COMPACT.

By using the element combination

$$R_g + R_s + R_d = \text{constant} \tag{33}$$

for the three transistors T1–T3 in Table I, it was illustrated that these transistors have different cutoff frequencies. This means that the element sum should not be minimized to obtain a maximized cutoff frequency, $f_{\max}$. It does indicate that the element sum should be optimized with the intrinsic part to produce a maximized cutoff frequency. This result is interesting since first-order theory indicates that the parasitic circuit elements should be minimized to provide the maximum $f_{\max}$. By calculating this sum for the real devices (data given in Table II), we observe that it is not the minimum sum that produces the highest $f_{\max}$ of these transistors.

VI. Conclusion

A powerful gain-partitioning approach that exploits the properties of various power measures has been presented. Previous implications by, among others, Trew [3] that the device structure of a compound transistor may be optimized to obtain a tuned high-frequency response have been verified. We have formulated the method by using concepts from basic circuit theory. Results presented here show that the requirements of maximizing the cutoff frequencies $f_{\max}$ and f_τ of a transistor are different in nature. Results indicate that minimized parasitic circuit elements maximize f_τ. A maximized $f_{\max}$, on the contrary, may be obtained if the interaction of parasitic and intrinsic circuit elements fulfills certain conditions. This means that parasitic circuit elements should be optimized, not minimized, in conjunction with the intrinsic element part of the transistor. The method presented here should be considered for use in conjunction with software that can specify the physical structure required to realize those circuit elements.

Appendix I
Partitioned Expression of Mason's Gain

The two-port z parameters of the network shown in Fig. 4, can be derived as

$$z_{11} = z_s + z_g + y^t_{22}/\Delta y^i \tag{A1}$$

$$z_{12} = z_s - y^i_{12}/\Delta y^i \tag{A2}$$

$$z_{21} = z_s - y^t_{21}/\Delta y^i \tag{A3}$$

$$z_{22} = z_d + z_s + y^i_{11}/\Delta y^i \tag{A4}$$

where

$$\Delta y^i = y^i_{11}y^i_{22} - y^t_{12}y^i_{21} \tag{A5}$$

and the superscript i denotes the intrinsic part of the device. Now, let the real part of the intrinsic device be denoted by $\mathrm{Re}(z^i_{lm}) = r^i_{lm}$, $l, m = 1,2$. Mason's gain may be written

$$U = \frac{|z^t_{21} - z^t_{12}|^2}{4\left[(R_g + R_s + r^t_{11})(R_d + R_s + r^t_{22}) - (R_s + r^t_{12})(R_s + r^t_{21})\right]}$$

$$= \frac{U_i}{1 + U_i(p_s + p_{g,d})} \tag{A6}$$

where

$$U_i = \frac{|z^t_{21} - z^t_{12}|^2}{4\left[r^t_{11}r^i_{22} - r^t_{12}r^t_{21}\right]} \tag{A7}$$

$$p_s = \frac{4R_s\left(r^i_{11} + r^t_{22} - r^i_{12} - r^t_{21}\right)}{|z^t_{21} - z^i_{12}|^2} \tag{A8}$$

$$p_{g,d} = \frac{4\left[R_g\left(r^t_{22} + R_s + R_d\right) + R_d\left(r^i_{11} + R_s\right)\right]}{|z^t_{21} - z^i_{12}|^2}. \tag{A9}$$

Appendix II
Derivation of the Partitioned Current Gain Equation

The current gain, A_i, is defined as the ratio of output current I_2 to the input current I_1 (Fig. 11); so that

$$A_i = \frac{I_2}{I_1}. \tag{A10}$$

When an impedance z_L is connected across the output, as shown in Fig. 11, the conditions existing at this port become constrained by the relation

$$V_2 = -I_2 z_L. \tag{A11}$$

In terms of the z parameters, we have, for the two-port network,

$$V_1 = z_{11}I_1 + z_{12}I_2 \tag{A12}$$

$$V_2 = z_{21}I_1 + z_{22}I_2. \tag{A13}$$

Eliminating now V_2 between the two voltage equations above and then solving for the current gain, we obtain

$$A_i = \frac{-z_{21}}{z_{22}+z_L}. \tag{A14}$$

Consider now the network topology shown in Fig. 4. The two-port z parameters can be derived as (see Appendix I)

$$z_{11} = z_s + z_g + y^i_{22}/\Delta y^i \tag{A1}$$

$$z_{12} = z_s - y^i_{12}/\Delta y^i \tag{A2}$$

$$z_{21} = z_s - y^i_{21}/\Delta y^i \tag{A3}$$

$$z_{22} = z_d + z_s + y^i_{11}/\Delta y^i \tag{A4}$$

where

$$\Delta y^i = y^i_{11}y^i_{22} - y^i_{12}y^i_{21} \tag{A5}$$

and the superscript i denotes the intrinsic element part of the device.

To obtain a compact notation, let us use the relationship between the impedance and admittance parameters:

$$z^i_{11} = y^i_{22}/\Delta y^i \tag{A15}$$

$$z^i_{12} = -y^i_{12}/\Delta y^i \tag{A16}$$

$$z^i_{21} = -y^i_{21}/\Delta y^i \tag{A17}$$

$$z^i_{22} = y^i_{11}/\Delta y^i. \tag{A18}$$

Thus, we obtain a current gain equation that can be written

$$A_i = \frac{-(z_s + z^i_{21})}{z_d + z_s + z_L + z^i_{22}}. \tag{A19}$$

This total current gain equation can now be manipulated to form an intrinsic current gain part and a parasitic current gain part. Depending upon the approach used, different analytical expressions can be obtained. However, it has been found that the procedure described below is well suited to illustrate the current gain partitioning approach. (It is numerically efficient and a side benefit is that the notation resembles that of classical feedback theory.)

Thus, the current gain may be written

$$A_i = \frac{-z^i_{21}(1+z_s/z^i_{21})}{z^i_{22}(1+(z_d+z_s+z_L)/z^i_{22})} \tag{A20}$$

and finally arranged to the form

$$A_i = \frac{(1+a)h^i_{21}}{1-bh^i_{21}} \tag{A21}$$

where

$$a = z_s/z^i_{21} \tag{A22}$$

$$b = (z_s + z_d + z_L)/z^i_{21} \tag{A23}$$

$$h^i_{21} = -z^i_{21}/z^i_{22}. \tag{A24}$$

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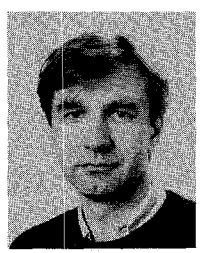

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